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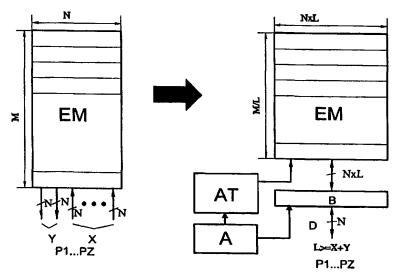
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(54) Title: SINGLE MEMORY WITH MULTIPLE SHIFT REGISTER FUNCTIONALITY



(57) Abstract: The present invention relates to a memory device comprising a memory (EM) having at least two predetermined register memory sections addressable by respective address ranges AS1-ASz) and at least one access port (P1-PZ) for providing access to said memory (EM). Furthermore, access control means (A) are provided for addressing said memory (EM) so as to operate said register memory sections as shift registers and to map shift register accesses of the at least one access port (P1 to PZ) to predetermined addresses in the global address space of the memory (EM). In this way, it is possible to combine a plurality of FIFO memories in a single addressable memory device. This implementation is favourable in view of power consumption and area. Furthermore, by introducing a buffer memory, a multi-port memory device can be replaced by a single-port memory device of the same capacity. This advanced implementation also provides a reduced cycle and access time.



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